



# UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, Virginia 22313-1450  
www.uspto.gov

| APPLICATION NO.  | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO.          | CONFIRMATION NO. |
|--|-------------|----------------------|------------------------------|------------------|
| 10/663,151   | 09/15/2003  | Peter Poechmueller   | INTECH 3.0-096 03 P<br>50757 | 2158             |
| 530  | 7590        | 10/13/2005           | EXAMINER<br>SONG, JASMINE    |                  |
| LERNER, DAVID, LITTENBERG,<br>KRUMHOLZ & MENTLIK<br>600 SOUTH AVENUE WEST<br>WESTFIELD, NJ 07090 |             |                      | ART UNIT<br>2188             | PAPER NUMBER     |

DATE MAILED: 10/13/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

10/663,151

Applicant(s)

POECHMUELLER, PETER

Examiner

Jasmine Song

Art Unit

2188

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 15 September 2003.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-21 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-21 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 15 September 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
  - ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date 01/12/04&03/04/05.
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_.

PD

## **Detailed Action**

### **Specification**

1. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

### **Drawings**

2. The drawings filed on 09/15/2003 have been approved by the Examiner.

### **Oath/Declaration**

3. The applicant's oath/declaration has been reviewed by the examiner and is found to conform to the requirements prescribed in 37 C.F.R. 1.63.

### **Information Disclosure Statement**

4. The information disclosure statement (IDS) submitted on 01/12/2004 and 03/04/2005 is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

### **Claim Rejections - 35 USC § 112**

5. The following is a quotation of the second paragraph of 35 U.S.C. 112:

Art Unit: 2188

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. Claim 11 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The language or term "post-fabrication stress testing" is not clear or distinct. This language is not defined in either the actual claim language or the specification. It is not clear as to whether the term "post-fabrication stress testing" is a well know term, an instructional test procedure in relationship to the refresh rate. It is not possible from either the specification or the claims to determine the scope of this language or to determine the metes and bounds of the claim.

### **Claim Rejections - 35 USC § 102**

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

8. Claims 1-4,6,8-15,17 and 20-21 are rejected under 35 U.S.C. 102(e) as being anticipated by Burgan., US 6,778,457 B1.

Regarding claims 1 and 12, Burgan teaches that a method of reducing a rate for refreshing a portion of a dynamic random access memory (DRAM), comprising:

storing information (it is taught as each of a plurality of substantially identical test memory cells includes a capacitor for storing charge representative of a stored logic state, col.2, lines 4-6) for distinguishing between a first portion of a DRAM (it is taught as a second portion of the plurality of test memory cells) requiring refresh at a first rate (col.8, lines 25-26) and a second portion of said DRAM (it is taught as a first portion of the plurality test memory cells) permitting refresh at a second rate lower than said first rate (col.8, lines 22-27); and

accessing said stored information to refresh said first portion at said first rate and to refresh said second portion at said second rate (it is taught as a monitor circuit for monitoring a charge storage ability of the first and second portions of the plurality of test memory cells).

Regarding claims 2 and 13, Burgan teaches said first portion and said second portion each include one or more segments of said DRAM (it is taught as each first portion and second portion include one or more test memory cells), and said information allows said first portion and said second portion to be distinguished on the basis of said segments (it is taught as each test memory cell having a capacitor for storing charge representative of a stored logic state and each of the test memory cells is refreshed at a different rate than other test memory cells).

Regarding claims 3 and 14, Burgan teaches that said first portion includes subportions (it is taught as the first portion includes a plurality of test memory cells), at least some of said subportions being physically discontinuous (see Fig.3).

Regarding claims 4 and 15, Burgan teaches that said subportions are wordline spaces of said DRAM and said information allows said first portion and said second portion to be distinguished on the basis of said wordline spaces (Fig.2 and col.2, lines 46-48).

Regarding claims 6 and 17, Burgan teaches the information is stored in said DRAM (col.2, lines 42-46).

Regarding claim 8, Burgan teaches that said information is stored on one or more fuses on an integrated circuit including said DRAM (it is taught as an integrated circuit memory 10 which includes memory array, control, decoders, sense amplifiers, and I/O circuits block etc as shown in Fig.1).

Regarding claims 9 and 20, Burgan teaches that said information further allows a plurality of portions numbering one to n of said DRAM (it is taught as a plurality of test memory cells) including said first portion and said second portion to be distinguished (the first and second portion is included in the DRAM) for refreshing said plurality of portions of said DRAM at a plurality of respective rates numbering one to n, and said stored

Art Unit: 2188

information is accessed to refresh said plurality of portions at said respective rates including to refresh said first portion at said first rate, to refresh said second portion at said second rate, and to refresh said nth portion at said nth rate(it is taught as each of the plurality of test memory cells is refreshed at a different rate than other test memory cells, col.2, lines 3-8).

Regarding claims 10 and 21, Burgan teaches that said information is stored in a space accessible through one or more wordlines of said DRAM (col.2, lines 39-48).

Regarding claim 11, Burgan teaches that said information is generated by post-fabrication stress testing of said DRAM (col.4, lines 15-17).

### **Claim Rejections - 35 USC § 103**

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

10. Claims 5 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Burgan., US 6,778,457 B1, in view of Klein., US 6,838,331 B2.

Regarding claims 5 and 16, Burgan teaches that said first portion is refreshed at said first rate and said second portion is refreshed at said second rate (see col.8, lines 22-27), Burgan does not teach that both said first portion and said second portion

operate in a mode selected from the group consisting of active mode and sleep mode. However, Klein teaches that both said first portion and said second portion (the memory cells in the DRAM) operate in a mode selected from the group consisting of active mode and sleep mode (col.2, lines 39-50).

It would have been obvious to the ordinary skill in the art at the time the invention was made to utilize the teachings of Klein into Burgan's memory system such as the memory cells in the DRAM operate in a mode selected from the group consisting of active mode and sleep mode because it will reduce the power consumed by a DRAM device during refresh in at least some operating modes without risking a loss of data stored in the DARM device (col.3, lines 36-54).

According, one of ordinary skill in the art would have recognized this and concluded that they are from the same field of endeavor. This would have motivated one of ordinary skill in the art to implement the above combination for the advantages set forth above.

11. Claims 7 and 18-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Burgan., US 6,778,457 B1, in view of Caulkins., US 6,473,355 B2.

Regarding claims 7 and 18, Burgan teaches the claimed invention as shown above (claims 1 and 12), Burgan does not teach that said information is stored in a non-volatile memory and accessed from said non-volatile memory for storage in said DRAM. However, Caulkins teaches said information is stored in a non-volatile memory and



Art Unit: 2188

accessed from said non-volatile memory for storage in said DRAM (col.3, lines 40-44 and col.5, lines 9-12).

It would have been obvious to the ordinary skill in the art at the time the invention was made to utilize the teachings of Caulkins into Burgan's memory system such as said information is stored in a non-volatile memory and accessed from said non-volatile memory for storage in said DRAM because the non-volatile memory can maintain data for extended periods of time without any power being supplied to the device (col.1, lines 36-38) and the non-volatile memory also provides the stability and security (col.3, lines 23-24).

According, one of ordinary skill in the art would have recognized this and concluded that they are from the same field of endeavor. This would have motivated one of ordinary skill in the art to implement the above combination for the advantages set forth above.

Regarding claim 19, Burgan teaches that said information is stored on one or more fuses on an integrated circuit including said DRAM (it is taught as an integrated circuit memory 10 which includes memory array, control, decoders, sense amplifiers, and I/O circuits block etc as shown in Fig.1).

## **Conclusion**

12. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Bae US 6310813 B1

Katayama et al US 6199139 B1

13. When responding to the office action, Applicant is advised to clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made. He or she must also show how the amendments avoid such references or objections. See 37 C.F.R. 1.111 (c).

14. When responding to the office action, Applicants are advised to provide the examiner with the line numbers and page numbers in the application and/or references cited to assist examiner to locate the appropriate paragraphs.

15. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jasmine Song whose telephone number is 571-272-4213. The examiner can normally be reached on 8:00-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabhan can be reached on 571-272-4210. The fax phone numbers for the organization where this application or proceeding is assigned are 571-273-8300.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-3900.

Jasmine Song



Patent Examiner

October 5, 2005

FOR

Mano Padmanabhan

Supervisory Patent Examiner

Technology Center 2100



**GARY PORTKA**  
**PRIMARY EXAMINER**